COMPREHENSIVE EXPERIMENTAL INVESTIGATION OF GATE CURRENT LIMITATION EFFECTS ON POWER GaAs FETs RF PERFORMANCES

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Abstract

This paper presents for the first time a detailed experimental investigation of gate current limitation effects on power GaAs FETs RF performances. This gate current limitation is entirely accomplished by dynamic compensation of the gate bias voltage. Effects of this current limitation on power added efficiency and output power performance have been examined through an extensive experimental investigation over the entire Smith chart. Comprehensive results are given and allow to determine the optimal resistor value needed for the gate current limitation. Thermal runaway problem is also taken into consideration when selecting the gate resistor.

Introduction

It is well known that excessive gate current is harmful to power GaAs FETs in terms of long term reliability [1, 2]. This current is generated when the positive peak of the RF signal at the gate of a FET is high enough to forward bias the gate junction in a pulsed pattern, or when the negative peak is low enough to force a pulsed avalanche current through the gate. The two events may occur alternatively from one half cycle of the RF signal to another. The gate and drain RF voltages and the gate-source static voltage dictate whether the forward (positive) pulsed current or the avalanche (negative) pulsed current will be predominant. A combination of these currents results in a DC current flowing through the gate.

The most widely used technique for limiting the amplitude of this DC gate current is to insert a series resistor in the DC path of the gate bias circuit, isolated from the AC path to avoid its interaction with the RF signal itself (see figure 1). This gate compensation resistor, R_G, converts proportionally the average gate current into a voltage drop in series with the gate voltage supply, and thus acts as an auto-compensation circuit. Depending on the input RF power, the resultant DC voltage applied to the gate is dynamically adjusted in order to reduce the gate current. This may result in considerable variations in the gate DC voltage. Increasing the value of R_G reduces these variations, but at the same time increases the chances to reach thermal runaway conditions when no RF signal is applied. This thermal runaway is due to the positive feedback of the leakage current between the gate and the source. Manufacturers generally recommend specific values for R_G for power MESFETs.

Although the principle of the gate current limitation has been described in the literature, its effects on the RF performances of the transistor in terms of power and power added efficiency during characterization or in circuit implementation have not been reported in the open literature. Furthermore, there is a lack of papers investigating the effects of the load impedance on the gate current variations. In addition, no publication reports an experimental or analytical approach to determine the optimal value of the compensation resistor, for a given specific power FET, which offers the best compromise between current limitation and thermal runaway conditions.

This paper presents a comprehensive investigation of the current limitation effects based on an experimental approach along with results obtained for a 3 Watt GaAs FET at 1.7 GHz (FLL351ME from FUJITSU). These results focus on the relationship and the interdependency between average gate current, input RF power level and the load impedance. Load-pull measurements are presented which, for the first time, present the dependency of gate current on the output load impedance. Effects of gate current limitation on output power and power added efficiency are also analyzed. The determination of the optimum value of R_G that minimizes the gate current without any risk of provoking thermal runaway is also discussed.

Study of the gate current limitation effects on output power and power added efficiency

An automated multi-harmonic active load-pull system similar to those presented in [3, 4] but operating

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at a higher power level has been developped for these experiments. Part of this system is illustrated in figure 2. The use of active loads allows to vary the reflection coefficient independently at the fundamental frequency, 1.7 GHz, while the reflection coefficient at the 3.4 GHz harmonic frequency is kept constant. In addition, the use of a six-port reflectometer [5] allows to precisely maintain a constant absorbed RF power ($P_{in}(f_o)$) by the FET during measurements. Good precision on $P_{in}(f_o)$ is an essential condition for accurate monitoring of the gate current as a function of the load impedance. A second reflectometer is used to measure the output power and the multi-harmonic load reflection coefficients $\Gamma_{out}(nf_o)$.

An FLL351ME power GaAs FET was tested in a class AB operation mode, I_{DS}= 12% I_{DSS}, for the purpose to search for an optimum power efficiency at an output power level condition close to the 1dB compression point. By maintaining an input power $P_{in}(f_o)$ constant at 250 mW ± 5 mW, and a constant reflection coefficient at 3.4 GHz ($\Gamma_{out}(2f_o) = 0.48\angle -17^o$) the output power and power added efficiency variations with respect to the load at 1.7 GHz ($\Gamma_{out}(f_o)$) were simultaneously measured when RG=0 Ω . The results obtained are shown in figures 3(a) and 3(b) respectively. The same measurements were performed using an RG=270 Ω and the results obtained are presented in figures 3(c) and 3(d). By comparing the results of both experiments we can deduce that the output power and power added efficiency performances are quasi-independent of the value of the resistor needed for current limitation purpose. Only a shift of 7 degrees and a slight decrease (by 3.3 %) in the magnitudes of the optimum load conditions are observed.

Dependence of gate current on the load impedance

Load-pull measurements on the average gate current have been performed for the same bias and input power conditions: I_{DS} = 12%I_{DSS} and Pin = 250mW. Figure 4(a) shows the variations of the gate current as a function of $\Gamma_{out}(f_o)$ with $\Gamma_{out}(2f_o)$ kept constant at $0.48\angle -17^o$ and $R_G = 0\,\Omega$. These results show a strong dependency of the average gate current on the fundamental load impedance. The extreme values of the gate current were -40mA (coming out of the gate) and +10 mA (entering the gate). These values fall far away from the range recommended by the manufacturer (-2mA to +4mA). Furthermore, a comparison based on figures 3(a) and 3(b) results reveals that this dependency is particularly pronounced when the output load impedance is near the region of optimum output power and power added efficiency. Moreover, the constant current contours that correspond to the average values of RF pulsed currents flowing through the gate, show that even for an output power not exceeding the 1dB compression point, the peak values of the RF gate currents can reach very high levels. Figure 4(b) shows the variation of the average gate current when a compensation resistor R_G = 270 Ω is used. The results prove that this value is high enough to limit the average gate current between -3 mA and +2 mA over the entire Smith chart.

Limitation of The Gate Current

Thermal runaway conditions may be provoked by a gate resistor when the transistor is biased and when no RF power is applied to its input. Any leakage current coming out of the gate will create a voltage drop across R_G, moving the bias towards V_{GS} = 0V condition. Consequently the drain current is increased and causes a rise in the device temperature. Depending on gate leakage current characteristics of the device as a function of temperature, this process might result in a continuous increase of the power dissipated in the device, which in turn might ultimately lead to the destruction of the device. A large value of R_G increases the sensitivity of the auto-compensation mechanism and thus ensures a better limitation of the gate current over a given range of input power. However, a large R_G value might induce the thermal runaway phenomenon in the absence of input RF power. Therefore a trade-off in the selection of R_G value has to be made.

In order to be able to determine the smallest value of R_G required for the limitation of the gate current within a given dynamic range of the input RF power, gate current measurements were performed on the GaAs FET with different values of R_G, while maintaining fixed load and static drain current conditions, ($\Gamma_{out}(f_o) = 0.636\angle 180^o$, $\Gamma_{out}(2f_o) = 0.48\angle -17^o$ and I_{DS}= 12%I_{DSS}), over a 10 dB dynamic range. It has been deduced that for these load and bias conditions, the maximum values of the average gate current specified for this transistor require that the input RF power range be limited between 340 mW and 400 mW for $R_G = 0\,\Omega$, between 0 mW and 500 mW for R_G = 100Ω and between 0 mW and 700 mW for R_G = 270Ω . These results are useful for the determination of the optimum value of R_G required for a given input RF power range. Besides, it has been determined experimentally that for this transistor the thermal runaway problems are expected to start up with R_G values of 500 Ω . This value fixes the upper limit for R_G. Thus for an input power range of 0 mW to 700 mW, R_G = 270Ω is the optimun value.

The $R_G = 0\,\Omega$ condition can be encountered in some applications, such as in MESFET device characterization and in MESFET amplifiers with

feedback control on gate biasing. The first application requires that the voltage applied to the gate, V_{GS}, be regulated. In this case there is no resistor in series with the gate supply voltage regulator. The second one concerns systems requiring that V_{GS} be controlled in a feedback loop as a function of any parameter uncorrelated to the gate current. Linearization methods using dynamic gate biasing with feedback control on V_{GS} [6] are typical examples. In such a case, any voltage drop across the gate resistor R_G due to an average gate current would result in an adjustment of V_{GS} through the control loop in order to compensate for this voltage drop and impose the required V_{GS} voltage to achieve the linearization purpose. Since V_{GS} is controlled via a feedback loop as a dependent voltage source, even if a series resistor R_G is physically present, the equivalent thevenin resistor seen from the gate is 0Ω. Therefore, it is expected that the gate current variations in the systems using regulated or feedback controlled V_{GS} exceed the safety limits and might present long term reliability problems.

Conclusion

An experimental investigation of the effects of gate current on RF performances of a power GaAs FET has been performed. It has been shown that the output power and power added efficiency performances are not altered by the gate current limitation. However a slight change in the optimum load conditions has been observed. For the first time load-pull measurements on gate current have been presented and show a strong dependency of the gate current on the output load impedance. Experimental measurements were used to select the value of the gate resistor that offers the best trade-off between current limitation and thermal runaway conditions.

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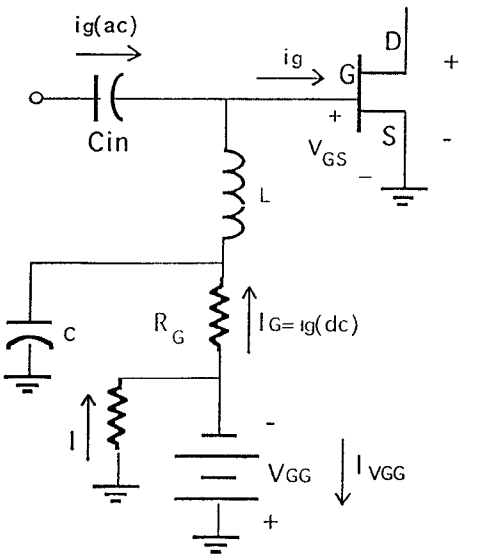

Figure 1: Equivalent circuit for gate biasing

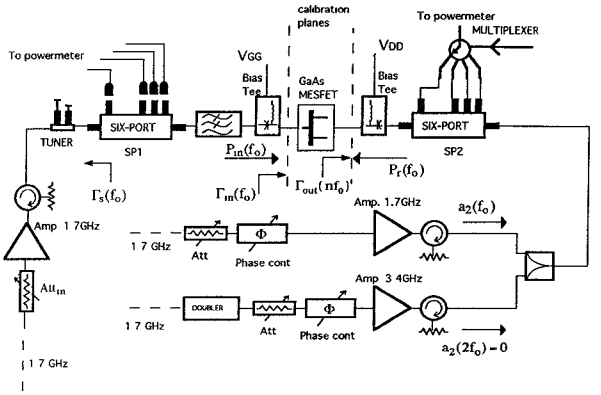

Figure 2: Multi-harmonic active load-pull system

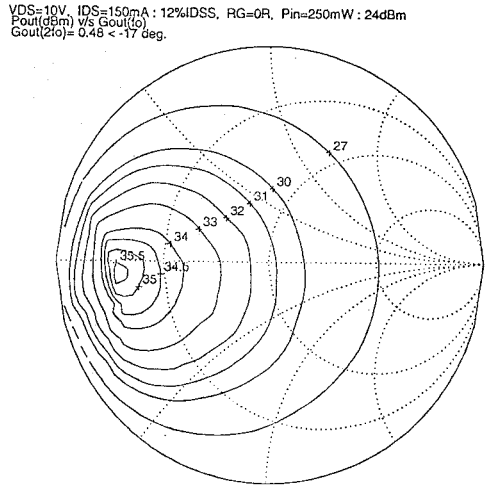

Figure 3(a): $P_{out}(f_o)$ v/s $\Gamma_{out}(f_o)$, $R_G = 0\ \Omega$

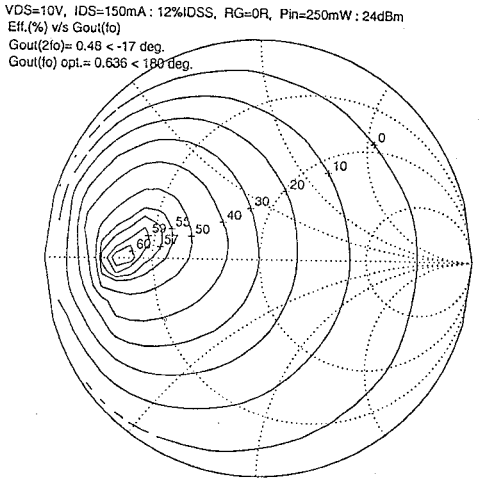

Figure 3(b): $Eff.(f_o)$ v/s $\Gamma_{out}(f_o)$, $R_G = 0\ \Omega$

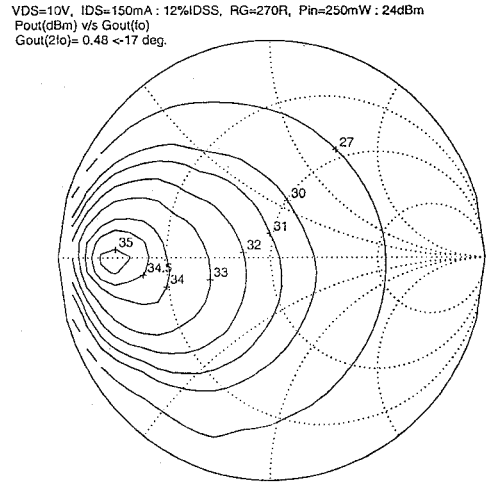

Figure 3(c): $P_{out}(f_o)$ v/s $\Gamma_{out}(f_o)$, $R_G = 270\ \Omega$

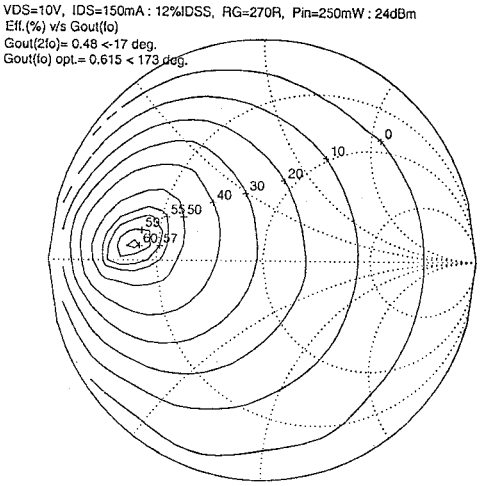

Figure 3(d): $Eff.(f_o)$ v/s $\Gamma_{out}(f_o)$, $R_G = 270\ \Omega$

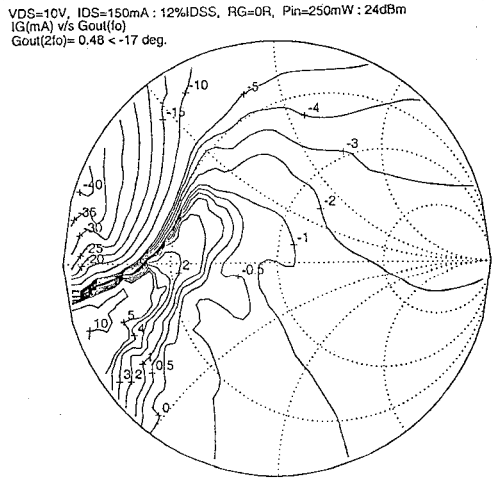

Figure 4(a): I_G v/s $\Gamma_{out}(f_o)$, $R_G = 0\ \Omega$

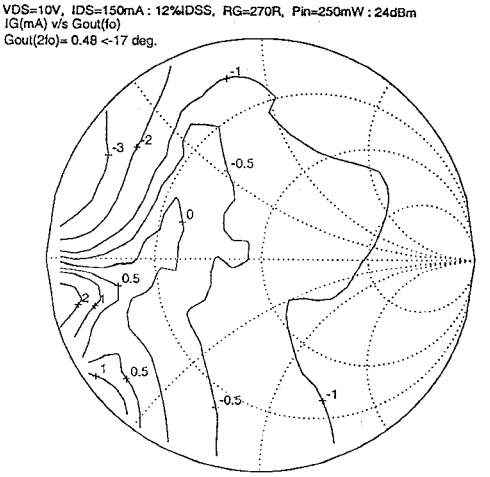

Figure 4(b): I_G v/s $\Gamma_{out}(f_o)$, $R_G = 270\ \Omega$